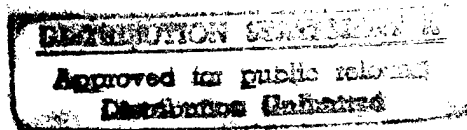**Rockwell**

September 3, 1996

Office of Naval Research
Ballston Tower One
800 North Quincy Street
Arlington, VA 22217-5600

Attn: Alvin Goodman, Code 312

Subject: High Speed Circuits and Packaging Technology for Advanced
Laser Altimeter Systems
Progress Report
Contract No. N00014-94-C-0112

In accordance with Contract No. N00014-94-C-0112, enclosed is the Progress
Report., 4/1/96 through 6/30/96.

ROCKWELL SCIENCE CENTER

*K C Wang*

K. C. Wang
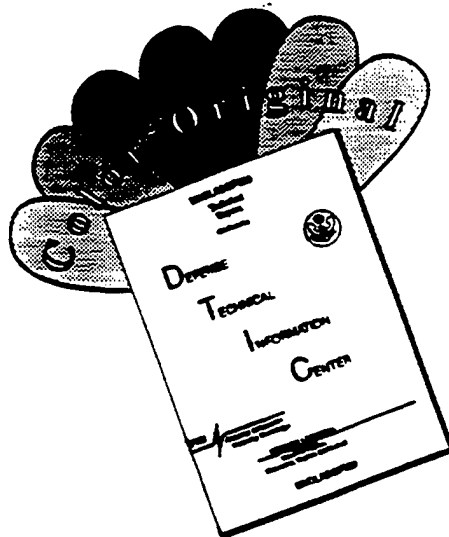Manager

Enclosure

KCW:gfm

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**High Speed Circuits and Packaging Technology**

**for Advanced Laser Altimeter Systems**

**Program Status Report**

4/1/96 through 6/30/96

To

Warner Miller (NASA Goddard SFC)

and Alvin Goodman (ONR)

By

Charles Chang , Dharmesh Jani, K.C. Wang,

Gerry Sullivan, and Edward Gertner

Rockwell International Science Center


Fu Ho and S.I. Long

Department of Electrical & Computer Engineering

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## 1.0 Introduction and Summary

In this report, progress on the high speed circuits and packaging technology for advanced laser altimeter systems is reported for the months of 1 April 1996 to 30 June 1996. During this time, significant progress has been made on both the 800 Ms/s and 3000 Ms/s data acquisition system. For the 800 Ms/s system, the ADC has been packaged and tested, the DEMUX substrate has been submitted for fabrication, and the packaged TIU is in the final stages of testing. The second cut schematic for the system has been designed and several PCB are presently being designed. The system timing of the 800 Ms/s system has been studied in great detail to assure the desired altimeter accuracy. For the high-speed system, the first test GaAs FIFO memory cells (512 x 1) have been fabricated and tested to 500 MHz. The memory design has been improved to make it less susceptible to switching noise. The second GaAs test cell has also be fabricated and is presently being tested. The CMOS FIFO is in the final design phase and should be submitted for fabrication in 3 months.

## 2.0 Progress on Data Acquisition System for Laser Altimeters
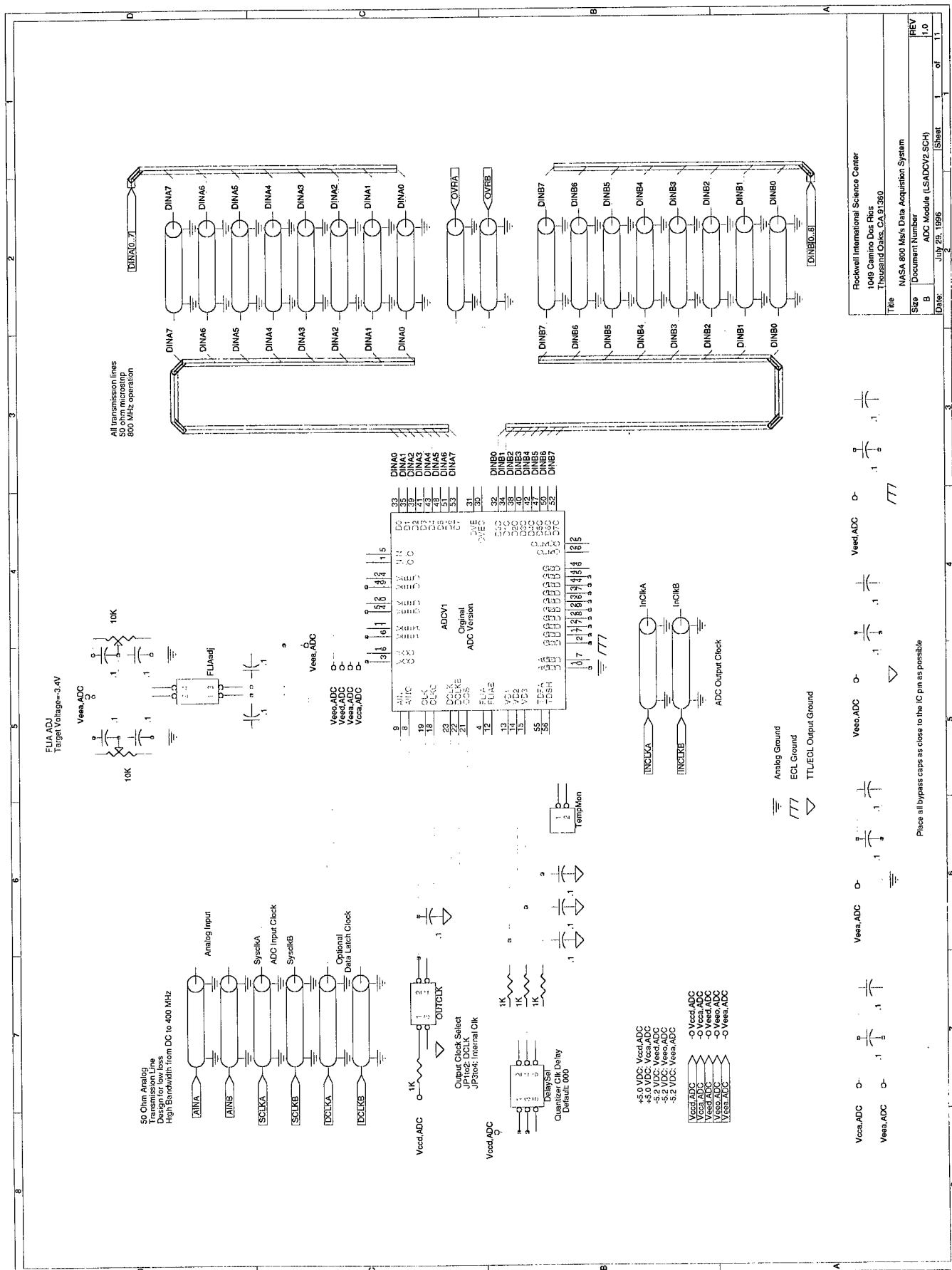
800 Ms/s system modifications

After the first cut design of the 800 Ms/s altimeter data acquisition system (presented in the previous quarterly report), Rockwell visited both Wei Fong and James Baker at NASA for review and comments. Since the date of the original proposal, NASA has updated some of the system requirements for the altimeter. Two primary changes that impact the 800 Ms/s design is the increase in desired memory and the change in computer interface requirements.
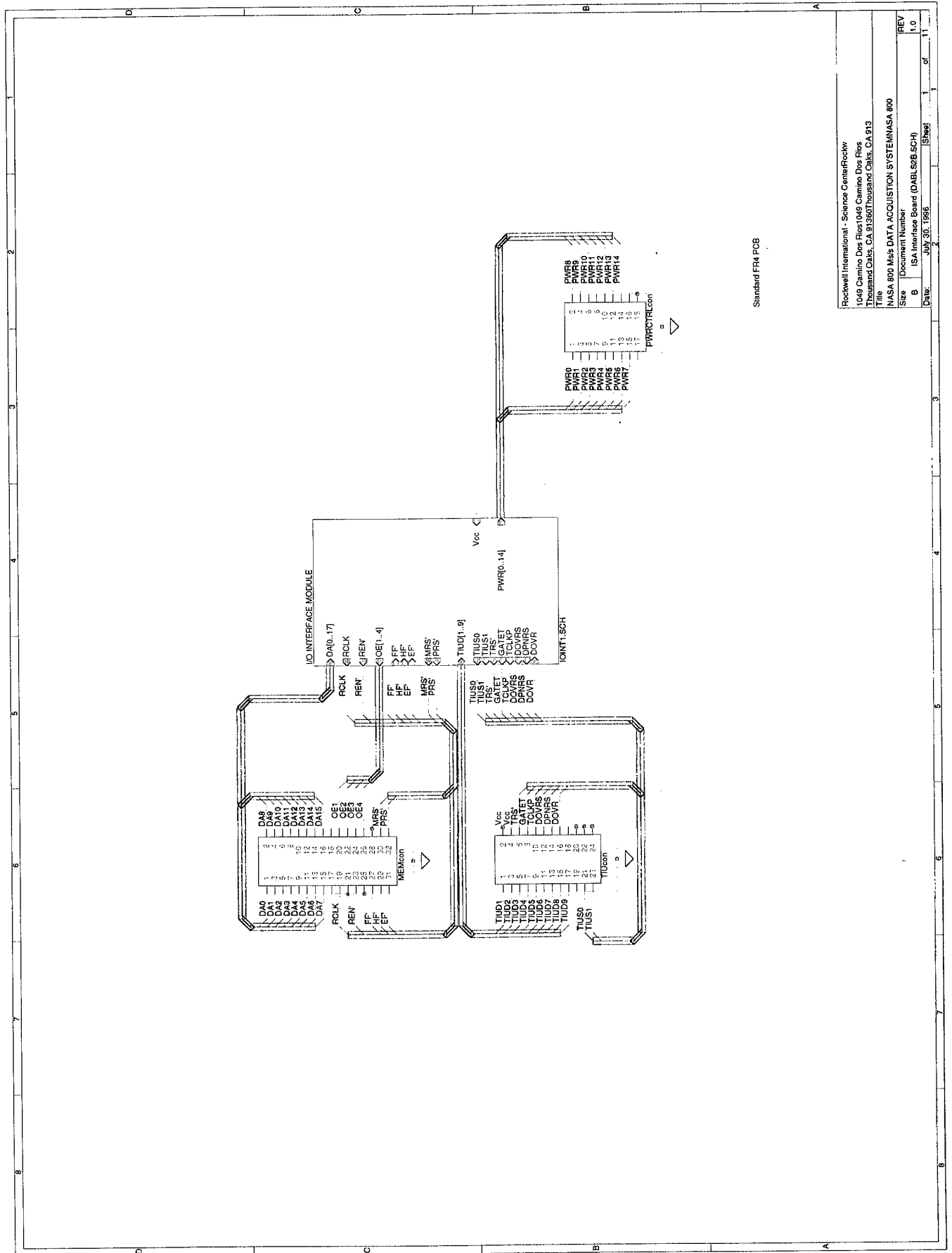
First, the initial design specification for the 800 Ms/s system required 8K ADC samples (8Kb of FIFO memory) since the digitized signal of interest was the return pulse itself. The new specifications require 64K samples (64Kb memory) since the duration of the signal of interest has increased. Fortunately, the 800 Ms/s system was designed with four 8Kb deep by 18 bit wide commercial FIFOs which meet the 64Kb memory depth with no modifications.

Second, the original plan employed the ISA bus as the interface between the 800 Ms/s system and the PC. After meeting, NASA system engineers will employ a direct high-speed microprocessor based interface to the 800 Ms/s system. Several changes were made to accommodate this requirement. In the original design, the ISA interface logic was on the same PCB as the core circuits (ADC, DEMUX, TIU, and MEMORY). In the new design, the core circuits reside on a separate PCB from the ISA interface logic. Rockwell will use the ISA interface logic board and a PC to test the system. NASA can directly connect to the data acquisition board (core) for their system development needs. From Rockwell's point of view, the ISA interface logic and a commercial ISA interface card minimizes the required hardware/software engineering time required to verify the performance of the 800 Ms/s data acquisition system.

Revised 800 Ms/s System Schematics

The revised schematic for the 800 Ms/s system is shown in figure 2.0-1 through 2.0-9. The design is broken into three printed circuit board. The main
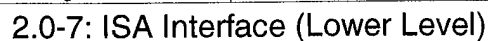
2.0-1: Data acquisition main schematic (Top Level)

2.0-2: Data acquisition- ADC sub-circuit

## 2.0-3: Data acquisition- DEMUX Sub-circuit

## 2.0-4: Data acquisition- FIFO Sub-circuit

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THOUSAND OAKS, CA 91360

Title: NASA LOW SPEED DATA ACQUISITION SYSTEM

| Size | Document Number | REV |
|------|-----------------|-----|
| B | Low-Speed FIFO Module (LSMEMV2.SCH) | 1 |
| Date: | July 30, 1996 | Sheet 5 of 11 |

2.0-5: Data acquisition- TIU Sub-circuit

2.0-6: ISA Interface (Top Level)

2.0-7: ISA Interface (Lower Level)

2.0-8: Power Control (Top Level)

2.0-9: Power Control (Lower Level)

data acquisition board is shown in fig. 2.0-1 through 2.0-5. The data acquisition board contains the ADC, DEMUX, TIU, FIFO memory, and the interface logic between the chips. Fig. 2.0-6 and fig. 2.0-7 contain the ISA interface which contains the logic that reads the FIFO and TIU as well as sets the many digitizer options. Fig. 2.0-8 and fig. 2.0-9 contains the schematic of the power management board. This board provides power to all of the chips as well as individual chip power control to minimize the overall power dissipation.

The ISA interface board and power management board has been designed and double-checked. The PCB is presently being designed and should be released for fabrication by Aug. 30th. The data acquisition board will be designed after further verification of the timing analysis that is expected to be completed by Aug. 30th.

800 Ms/s timing analysis

Fig. 2.0-10 shows a block diagram of the data acquisition board. Due to the various required logic levels, several ECL-TTL, CML-ECL, and ECL-CML converters were needed to interface to the chips. Since each chip contributes to the propagation delay, a detailed timing analysis was necessary to verify the accuracy of the acquisition system. The primary objectives are 1) to make sure that the TIU stop and FIFO data write occurs without any loss in time (+/- 1 clock cycle of the 800 MHz TIU clock), 2) to determine what sample the ADC/DEMUX first writes into the FIFO memory, and 3) to make sure the setup and hold times for the FIFO are meet. Errors in any of the above cases may result in the loss of accuracy due to uncertainty in the timing relationship between the data in the FIFO and the coarse count in the TIU.
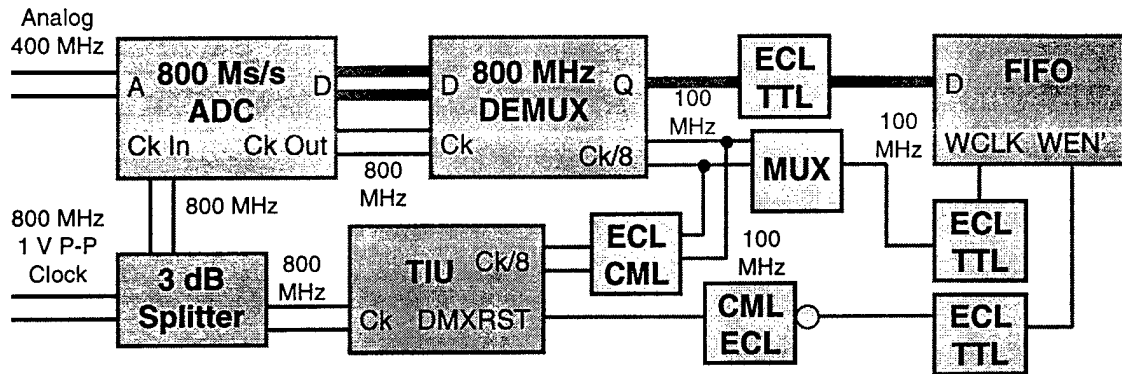
Fig. 2.0-10: Data Acquisition system simplified block diagram.

The period of the output clock is a fast 10 ns. As it turns out, the propagation delay of the commercial level converters (ECL-TTL, ECL-CML, and CML-ECL) are a significant portion of that 10 ns. Furthermore, the propagation delay varies as a function of actual gate loading and temperature which can vary the propagation delay by as much as 2-3 ns. When the propagation delay loading effects and the cascading effects of several different converters are taken into account, the overall variation can be significant. To study the delay variation impact on the system, detailed timing analysis for the 800 Ms/s system was carried out. After careful consideration, there exists four cases that can be studied to minimize the propagation delay effects. Fig. 2.10-11 diagrams the four cases.
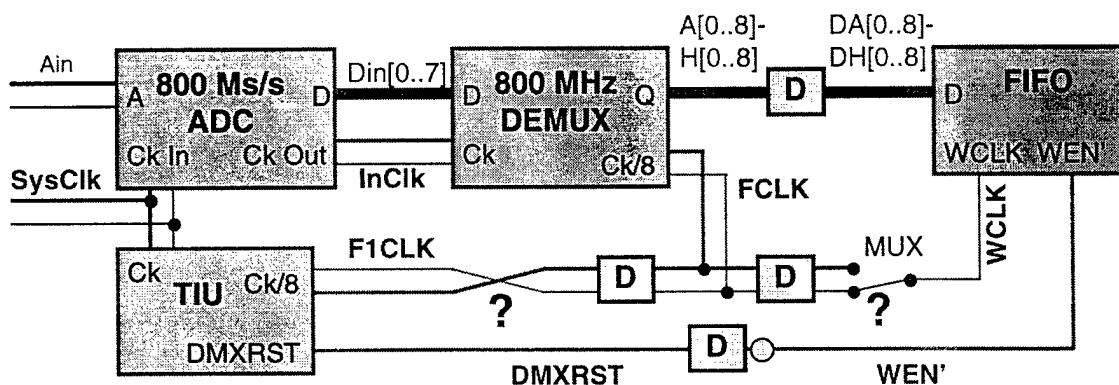


Fig. 2.0-11: Data Acquisition system with timing skew points shown

From a hardware point of view, the timing diagram can be skewed by the polarity of the DEMUX output clock (FCLK) going into the TIU (F1CLK). This skew point wired into place. The second skew point is the selection of the FIFO clock phase (WCLK) from FCLK. For flexibility, this is selected with an ECL mux. The four case can be summarized as:

Case 1: FCLKB to WCLK & FCLKB to F1CLKA
Case 2: FCLKA to WCLK & FCLKB to F1CLKA
Case 3: FCLKB to WCLK & FCLKA to F1CLKA
Case 4: FCLKA to WCLK & FCLKA to F1CLKA

Although the analysis was carried out for all four cases, only case 1 and three will be presented since the initial design will wire FCLKB to F1CLKA.
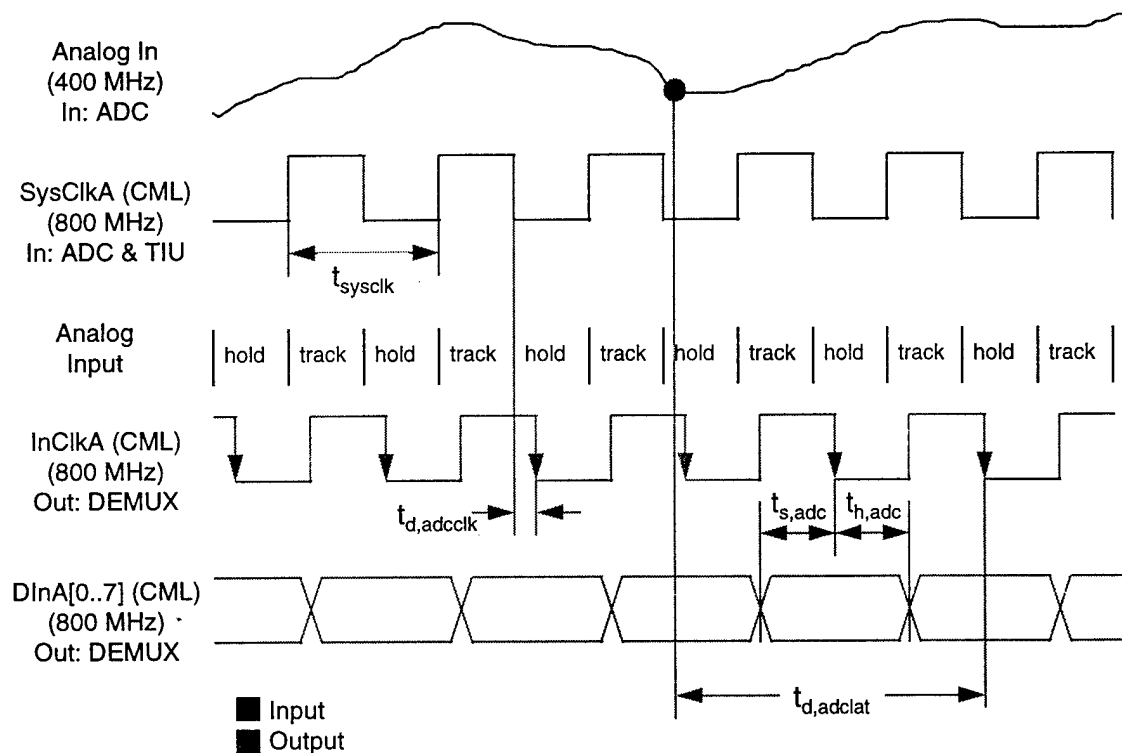
Fig. 2.0-12: ADC Timing Diagram

Fig. 2.0-12 shows the timing analysis for the ADC. The clock phase relationship to the data is shown. At this time, the latency of the ADC ($t_{d,adclat}$) has not been measured. From a system point of view, the constant latency does

not contribute to the 'error of the system, it just adds a know offset to the measured data.
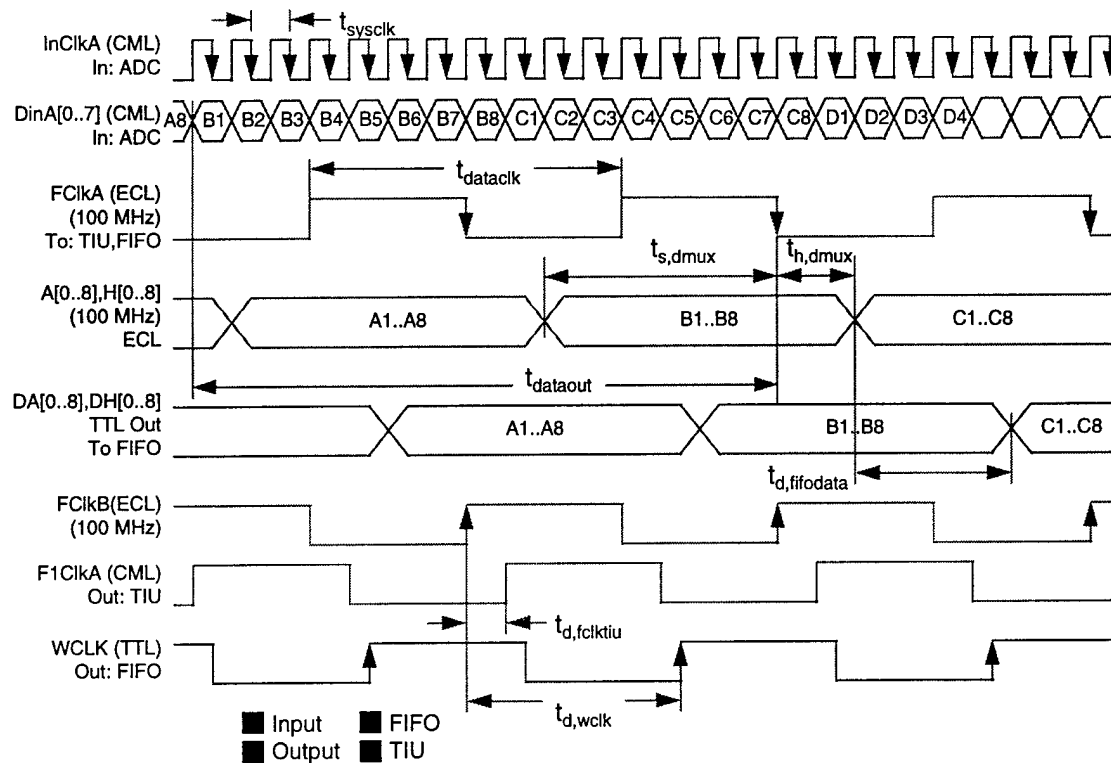


Fig. 2.0-13: DEMUX Timing Diagram

Fig. 2.0-13 shows the timing diagram for the DEMUX. The output phase relationship between the DEMUX clock (FCLKA) and data has been verified through low-speed DEMUX testing. In the DEMUX, there are 15 clock cycles from the first data of eight latched to the falling edge in FCLKA that frames the data output. This delay is constant so it does not impact the accuracy of the system and the 15 clock cycle delay actually simplifies the system design (otherwise, it may be possible to lose some of the data). The DEMUX data to the FIFO data is delayed by one ECL-TTL level converter. The WCLK is derived from a delayed version of FClkB. Unlike the data, WCLK is delayed by both the ECL mux and the ECL-TTL level converter. This maximizes the data setup time and minimize the data hold time as required by the FIFO; however, the rising edge of WCLK is pretty close to the end of the data. By selecting the other

option in the mux (WCLK from FCLKA), the edge is shifted back by 5 ns. The clock to the TIU (F1ClkA) is delayed from WCLKB by one ECL-CML converter.
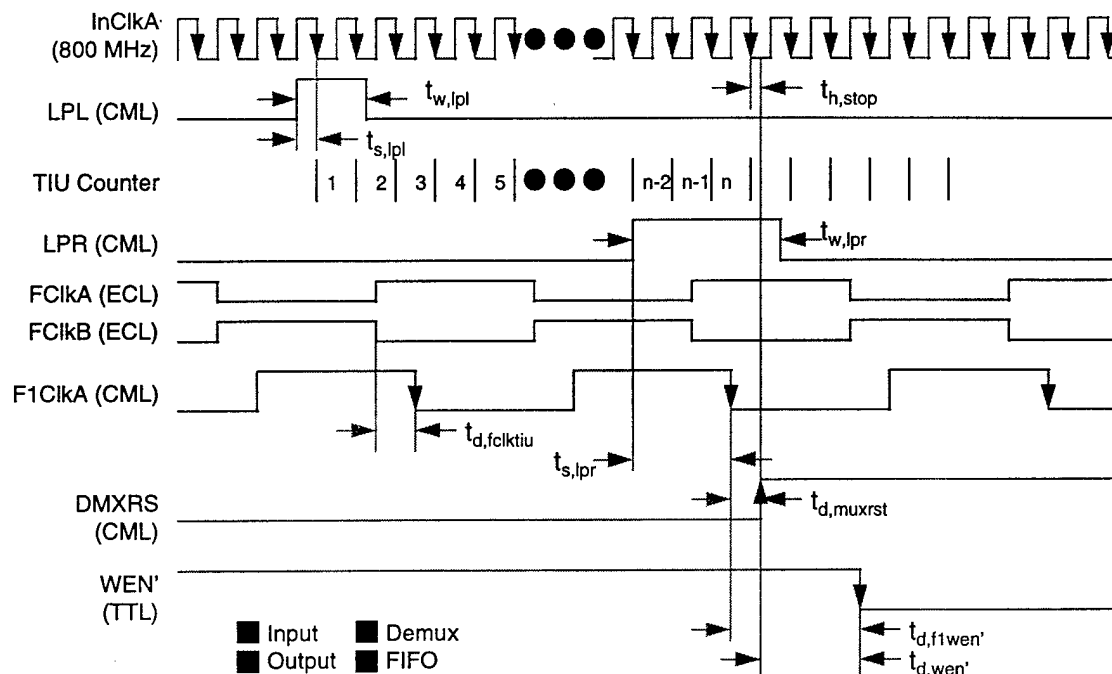


Fig. 2.0-14: TIU Timing Diagram

Fig. 2.0-14 shows the timing diagram for the TIU. This timing diagram was verified by both low-speed testing and from the schematic. Upon the first falling edge of the 800 MHz InClkA after the launch pulse leave (LPL) signal, the TIU coarse counter will count. For the non-resetable DEMUX, upon the first falling edge of F1ClkA (100 MHz Clock) after the receipt of the launch pulse return (LPR), the coarse counter will stop and the DMXRS reset signal will go high. This CML signal is inverted and converter to TTL (CML-ECL and ECL-TTL) and is used to enable the FIFO memory (WEN'). In general, the LPL and LPR signals are asynchronous to the InClkA. As a result, if the LPL or LPR setup/hold times are not meet, then the next clock period will start/stop the system. This results in the unavoidable one period uncertainty. Due to the high-speed nature of HBT circuits, the expected setup and hold times of the TIU are very short to minimize these errors.
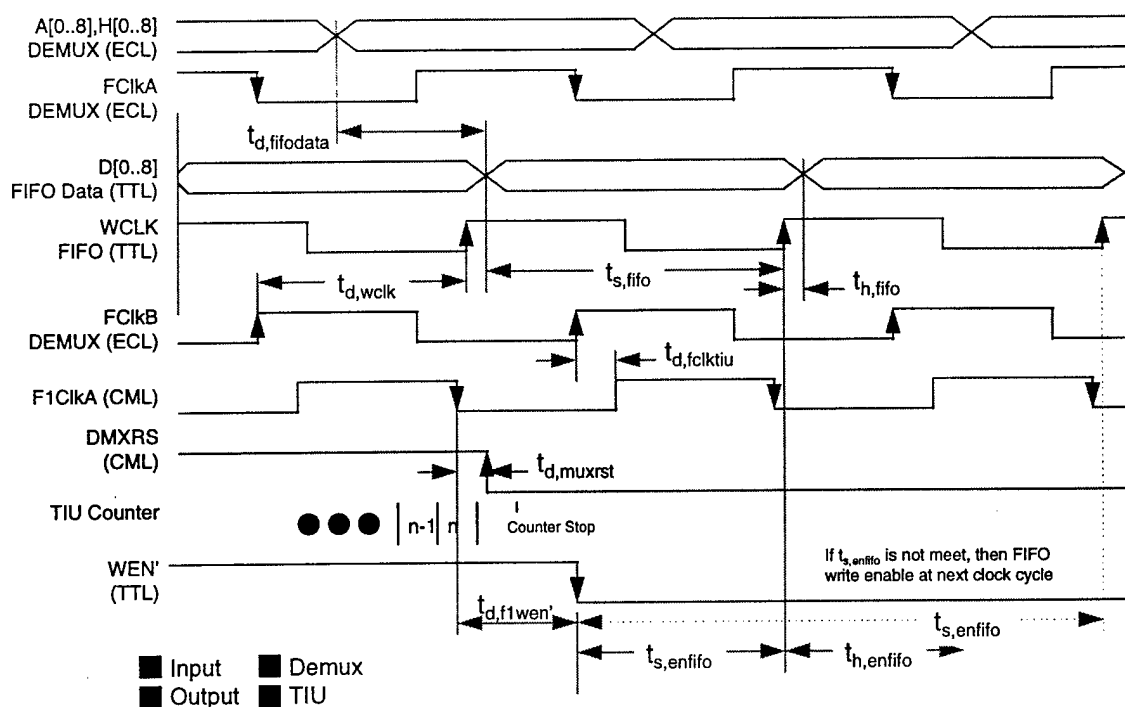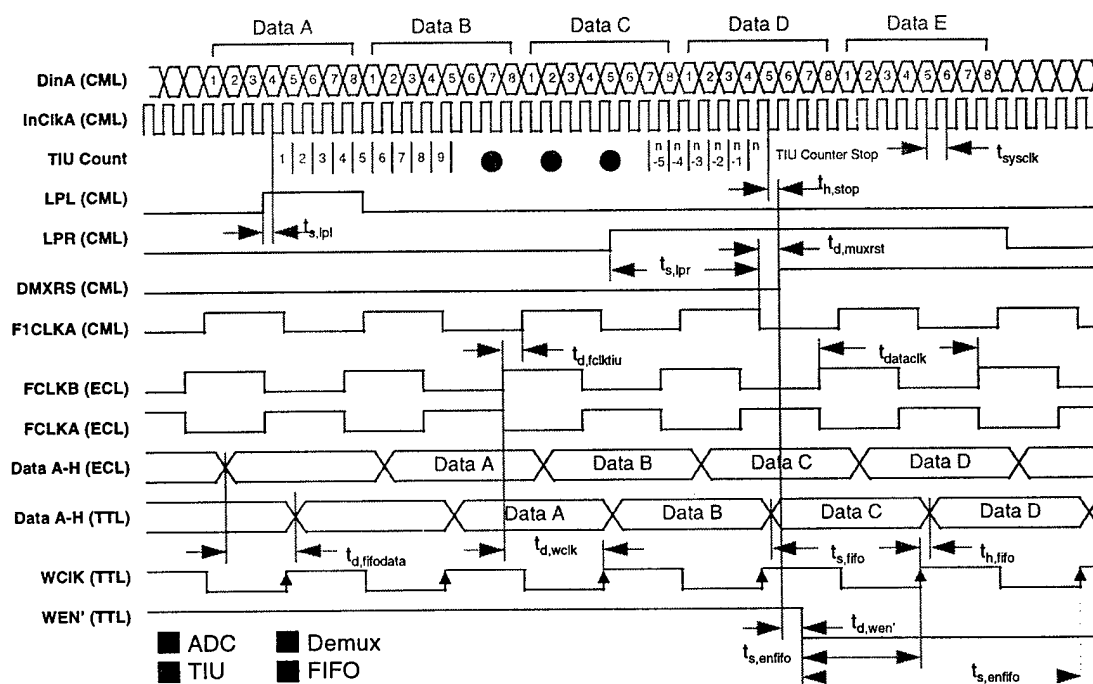
Fig. 2.0-15: Memory Timing Diagram



Fig. 2.0-16: Case 1: Overall Timing Diagram

Fig. 2.0-15 shows the timing diagram for the memory. This figure shows that the WEN' signal from the TIU must meet the setup time of 3.5 ns ($t_{s,enfifo}$)

before the rising edge of WCLK. If this is not meet, then the next DEMUX output data will be written into the memory. This setup time can be shifted by 5 ns when the input phase of the FCLKA to the TIU is shifted by 180° (case 2 & 4). With regards to the data/WCLK phase relationship, the setup/hold time for this memory is 3.5 ns/ 0 ns which is maximized in case 1.
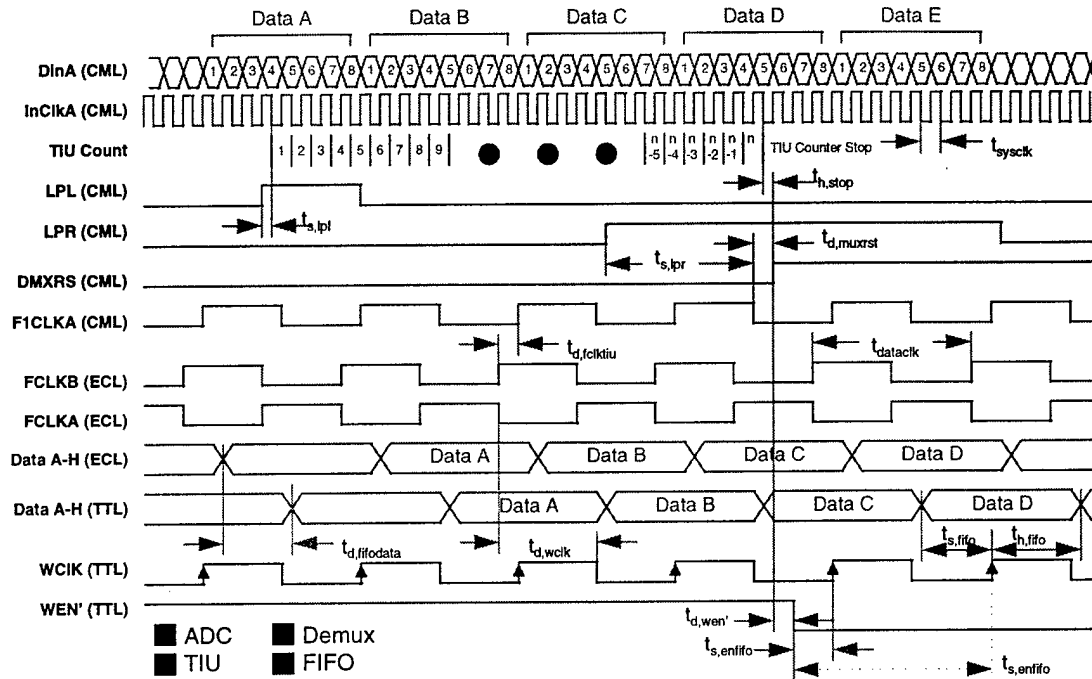


Fig. 2.0-17: Case 3: Overall Timing Diagram

Fig. 2.0-16 shows the overall timing diagram for the first case. In the diagram, the TIU stops during the DEMUX output cycle D at the fifth byte (D5). D5 is the first meaningful data from the ADC and any data after D5 must be maintained. In the best of cases, $t_{d,wen'}$ is short and the setup time is meet by the first rising edge of WCLK with respect to WEN'. In this case, the first data written into the FIFO is C1-C8. Here, the first 12 bytes read from the FIFO (C1-C8, D1-D4) is not meaningful can be discard. In the worst of case, the setup time is not meet for cycle C and will definitely be meet for cycle D. In this case, the first 4 bytes (D1-D4) written to the memory can be discarded. In either case, no meaningful data is lost and the position of the fist meaningful full data with respect to the TIU count is not lost and the accuracy of the system is maintained. In principle, the system will always read either Data C or Data D as

the first bytes written into the FIFO. The actual data (C or D) depends on the actual loaded propagation delays and process variation of the circuit after it is built (the propagation delay spread as published from the data sheets span both cases).

Fig. 2.0-17 shows the overall timing diagram for case three when the FIFO DEMUX selects FCLKA instead of FCLKB. In this case, the WCLK edge is shifted closer to the middle of the output data. If in case 1, the edge is too far to the left, this should by an increase in the data hold time at the expense of the data setup time. In this case, it is most likely that DEMUX cycle C will be missed and data cycle D will be the first data written into the FIFO.

Using published delay variations in the conversion circuits, the best and worst case delays are shown below.

Worst case propagation delays

| Max Dev | Fifo Enable | | FIFO Write | |
|---|---|---|---|---|
| | C[0-8] | D[0-8] | Ts,fifo (ns) | Th,fifo (ns) |
| Case 1 | 2.3 | 12.3 | 9.4 | 0.6 |
| Case 3 | -2.7 | 7.3 | 4.4 | 5.6 |

Best case propagation delays

| Min Dev | Fifo Enable | | FIFO Write | |
|---|---|---|---|---|
| | C[0-8] | D[0-8] | Ts,fifo (ns) | Th,fifo (ns) |
| Case 1 | 4 | 14 | 8 | 2 |
| Case 3 | -1 | 9 | 3 | 7 |

In both cases, the setup/hold time for the FIFO data and the FIFO enable is 3.5 ns/0 ns. With the worst case, the FIFO data write setup time is always meet in both cases 1 and 3. Furthermore, the worst case will get block D as the first eight bytes. With the best of cases, the data write setup time can not be meet in case 3 and case 1 will work with block C as the first eight bytes. In general, the expectant case will be between the two and there is no guarantee that the enable or data setup time will not fall at the edge of the setup time. If so, the ability to electronically choose between case 1 and 3 increase the robustness of the system against errors. During system test, the optimal case will be

determined that gives the greatest setup/hold margins over the expected temperature/process variations.

At present, the results of the timing analysis is being double checked with the data acquisition system schematic. The PCB design is expected to begin by the first week of September.

800 Ms/s system development

The PCB level heatsink for the ADC and DEMUX has been specified. The DEMUX will use a standard heatsink with a 40 x 40 mm$^2$ fan for minimal thermal resistance. For the ADC, a commercial heatsink will be machined for use with the custom ADC package. It will also be cooled with a fan for test purposes. For flight purposes, the thermal management issues can be addressed with more elaborate vacuum compatible heat spreader design at a later date.

At present, the power supplies, rack mount case, and other necessary items have been specified and ordered.

## 2.1 ADC and DEMUX Testing and Fabrication

Wafer level functionality test of ADCs from lot 40047 was done at the Newbury park facility. The testing was done with input clock at 800MHz and input signal at 7.7MHz. In input clock frequency reflects the clock rate of the 800 Ms/s system. Following is the summary of the test results obtained on 5 wafers.

| Wafer# | ADC Probed | Working ADCs | Yield (%) | Avg. ENOB |
|--------|-----------|--------------|-----------|-----------|
| 1 | 23 | 21 | 91 | 5.4 |
| 2 | 48 | 32 | 67 | 5.3 |
| 5 | 43 | 37 | 86 | 5.6 |
| 7 | 43 | 37 | 86 | 5.7 |
| 12 | 39 | 27 | 69 | 5.7 |
| All Wafers | 196 | 154 | 79 | 5.5 |

Wafer level functionality testing of DEMUX was carried out at Science Center to identify the working dies. The testing focused on determining if all 72

Output Clock

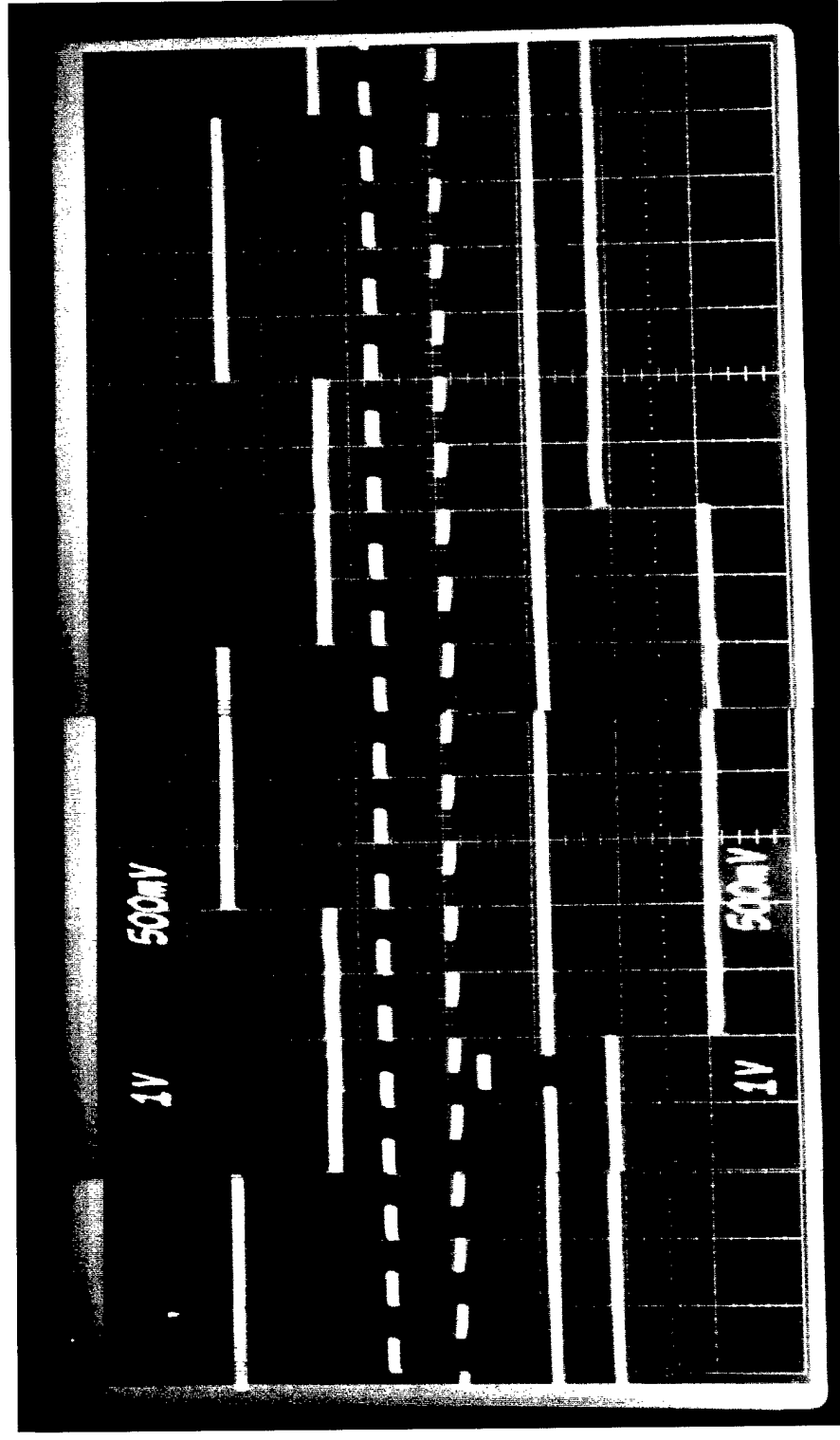Input Clock

Data In

Data Out
(channel A)

Fig. 2.1.1 Demux Test Waveforms

outputs were functional. The test results for an input clock of 10 MHz is summarized below.

| Wafer# | Demux Probed | Working Demux | Yield (%) |
|--------|--------------|---------------|-----------|
| 1 | 7 | 6 | 85.7 |
| 2 | 5 | 2 | 40 |
| 5 | 16 | 11 | 69 |
| 7 | 17 | 15 | 88 |
| 12 | 19 | 7 | 37 |
| All Wafers | 41 | 64 | 64 |

The Fig.2.1.1 shows the phase relationships of DEMUX input clock, output clock, input data, and output data. The results verify that there are 15 clock cycles between the first input data (of eight) to the output.

At present, wafer 7 and wafer 1 have been thinned to 7 mils and is presently being diced.


## 2.2 ADC and DEMUX Packaging Design

2.2.1 ADC Package Design

The Rockwell custom designed ADC package was successfully fabricated by Stratedge. A microphotograph of the packaged ADC is shown in fig. 2.2.1-1. In that figure, the ADC is indium soldered to the package for minimum thermal resistance. The die cavity to die spacing was kept short for minimum bondwire inductance. On-chip capacitors (epoxied and wirebonded) are used to de-couple the power supply. For the initial run, five ADCs were packaged, tested, and shown to be functional. At present, the epoxy lids are being attached to the package which would complete the ADC packaging process.

To test the ADC non-destructively, an ADC test-fixture was designed and fabricated. The test fixture PCB consists of a 10 mil thick Duriod 6006 layer on 48 mil glass-epoxy layer. The Duriod layer contains the high-speed low-loss transmission lines and the ground plane. The FR4 provides mechanical rigidity to the Duriod as well as low-speed signal routing. Fig. 2.2.1-2 shows a photograph of the top of the test fixture. The analog signals are brought into the test fixture via SMA connectors good to 18 GHz. The digital outputs and clocks
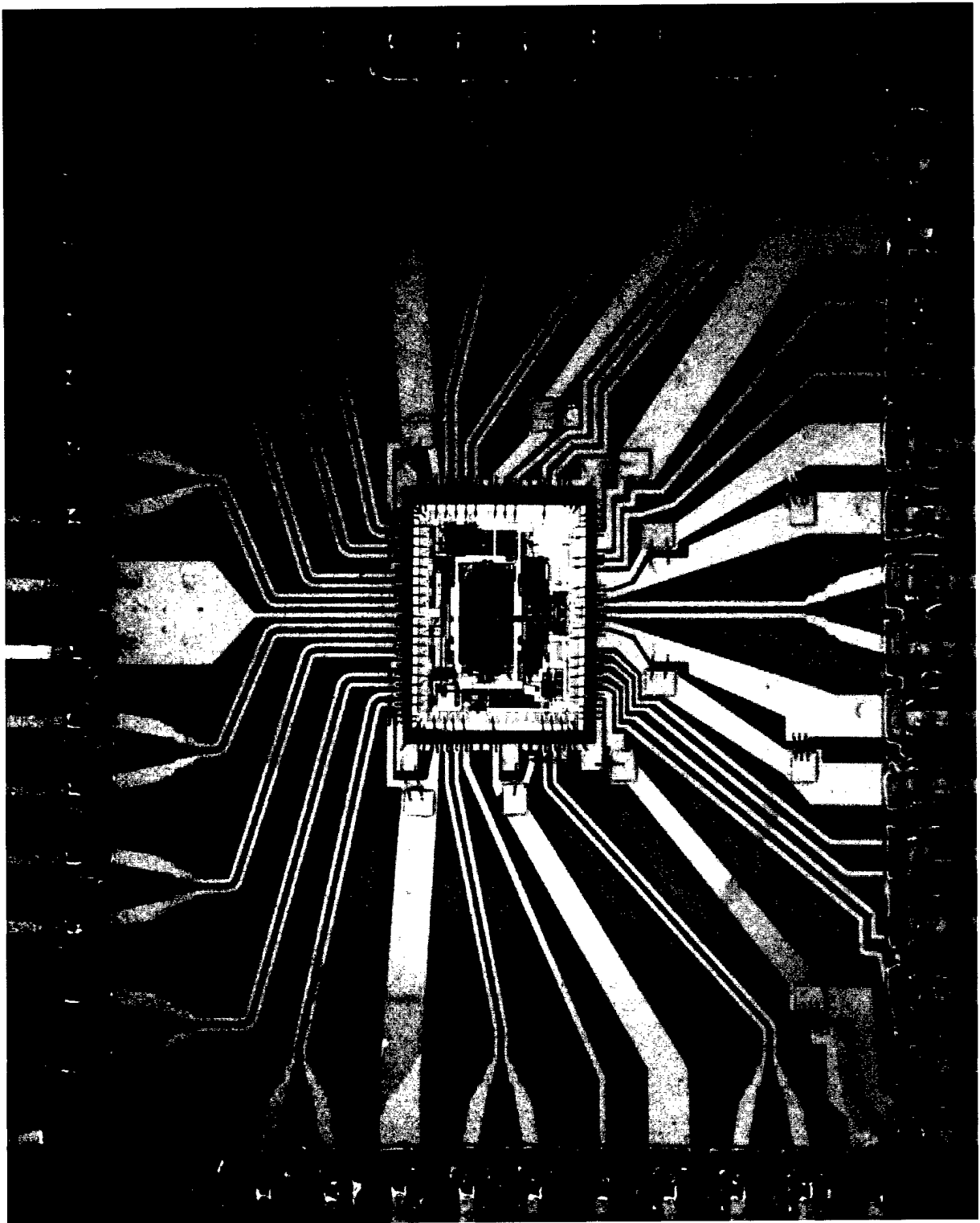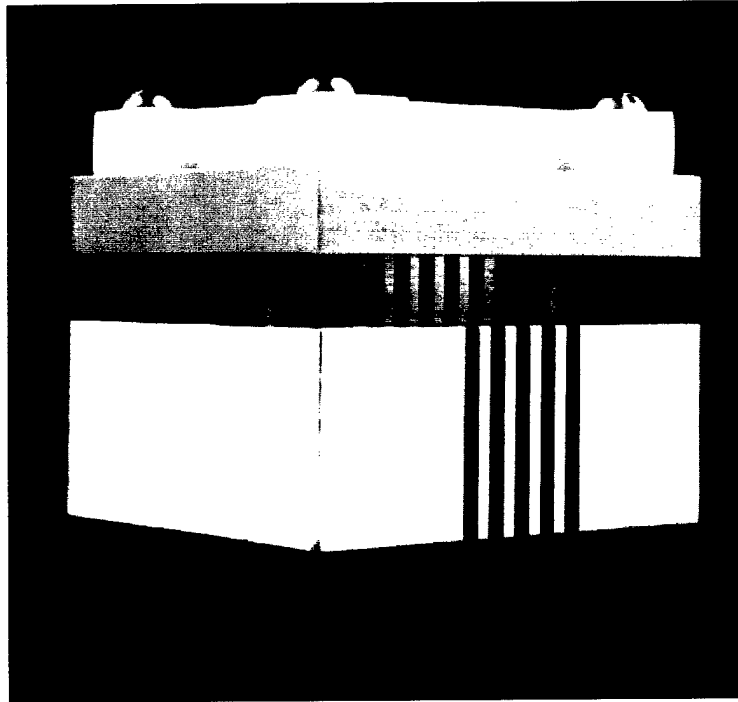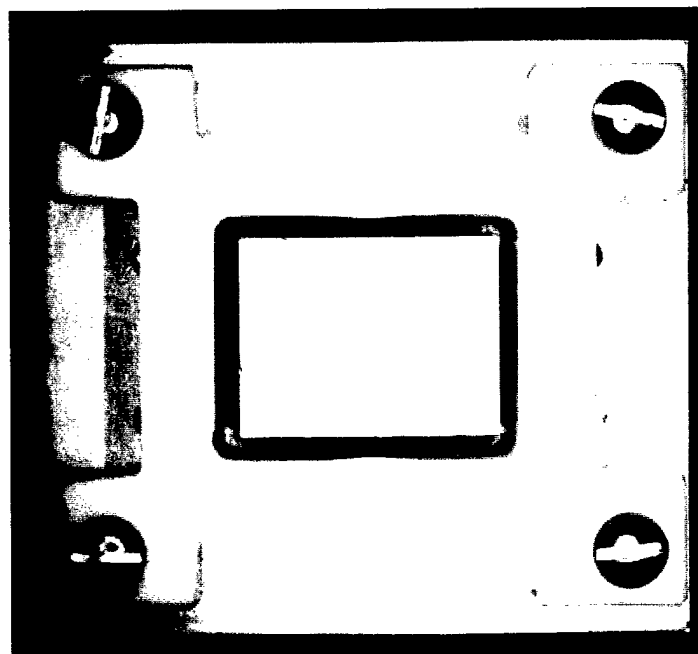
Fig. 2.2.1-1 Microphotograph of the packaged ADC showing the ADC die, de-coupling capacitors, and custom-designed package with differential coupled microstrip transmission lines.

(A)



(B)

Fig 2.2.1-3: ADC Testfixture chip mount a) Quarter view showing the spring loaded heat sink b) Top view showing the Teflon package lead clamp
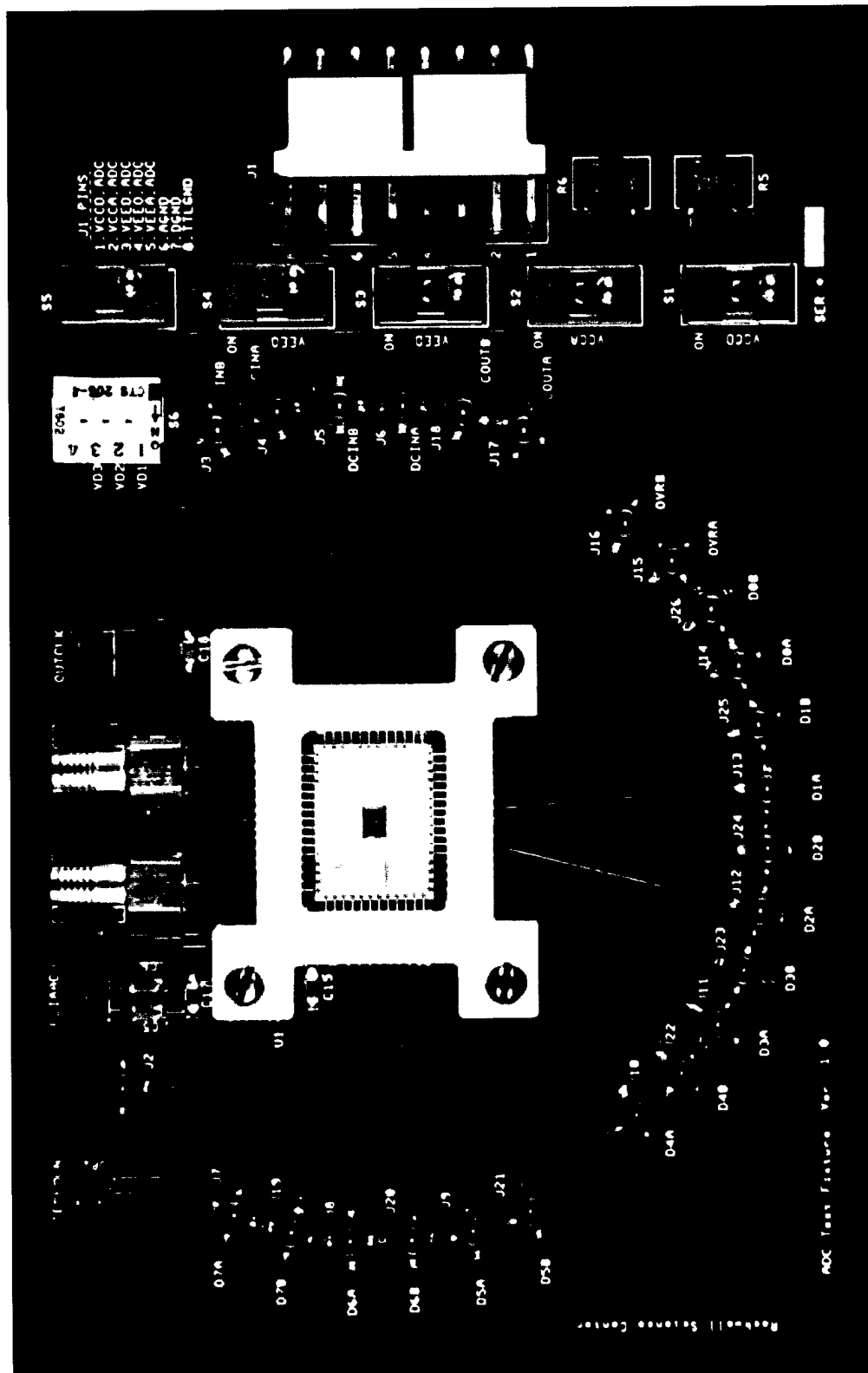
Fig. 2.2.1-2: Non-destructive ADC Testfixture PCB (Top View)

are brought in to and out of the test-fixture through surface mount OSMT connectors. These small OSMT connectors (good to 6 GHz) allow a high connector density which minimizes the transmission line length. Commercial OSMT to SMA cables were purchased to interface with SMA based test equipment. The test fixture uses a custom designed ADC holder shown in fig. 2.2.1-3. The holder serves two purposes. First, the Teflon clamp sandwiches the package lead frame to the PCB for non-destructive testing. Second, a spring load heatsink contacts the heat-spreader in the packaged to lower the temperature of the ADC during test.

Initial tests showed that the test fixture and ADC functioned with up to a 2 GHz input clock (995 MHz analog input/ 2 GHz output clock). The frequency is presently limited by the test equipment. For two of the packaged ADC, the effective number of bits is around 5. For these initial tests, the quantizer delay has not been optimized. At this point, the loss in ENOB may be due to the test fixture, package, and/or non-optimal quantizer delays. Further tests will concentrated on increasing the ENOB will be necessary to analyze the packaged ADC in greater depth.

2.2.2 DEMUX Package Design

Fig. 2.2.2-1 illustrates the final design of the DEMUX transmission line substrate that was released for fabrication. The modification include pool-table pocket cutouts in the corner of the DEMUX die cavity to accommodate the corners of the chip with minimum die to die-cavity spacing. Other modifications include a 2 mil set back of all of the traces from the edge of the alumina substrate. The design was submitted for fabrication and due back Aug. 28.
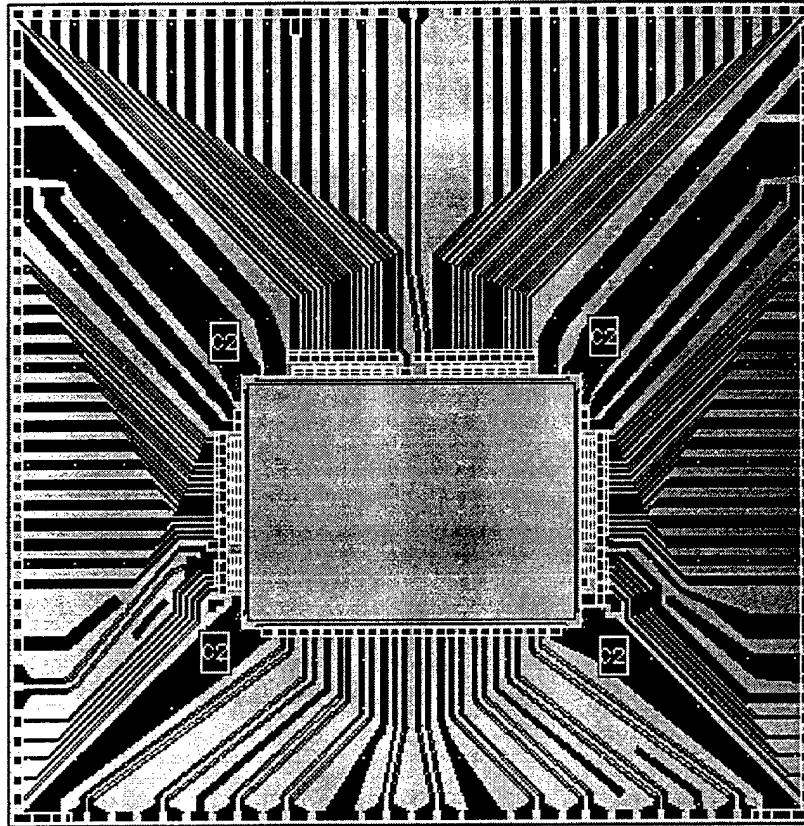
Fig. 2.2.2-1: Layout of the DEMUX substrate

## 2.3 Time Interface Unit TIU

TIU is used for registering the laser return pulse. It's main function is to generate a coarse count of time of flight of laser pulse and to generate the FIFO read signal when it registers the laser pulse return.

TIU has been tested on wafer at input clock of 5GHz. The working TIUs have been identified and packaged in 32 pin MSI package as shown below along with TIU specifications.

The first version of TIU had a error in resistor layout which lead to lower voltage swings for the push pull output stage. Thus the output transistors don't turn off completely. This results in higher current draw from $V_{cc}$ supply increasing the power dissipation in the output buffers. This error has been corrected in the subsequent TIU layouts. Following table summarizes TIU versions.
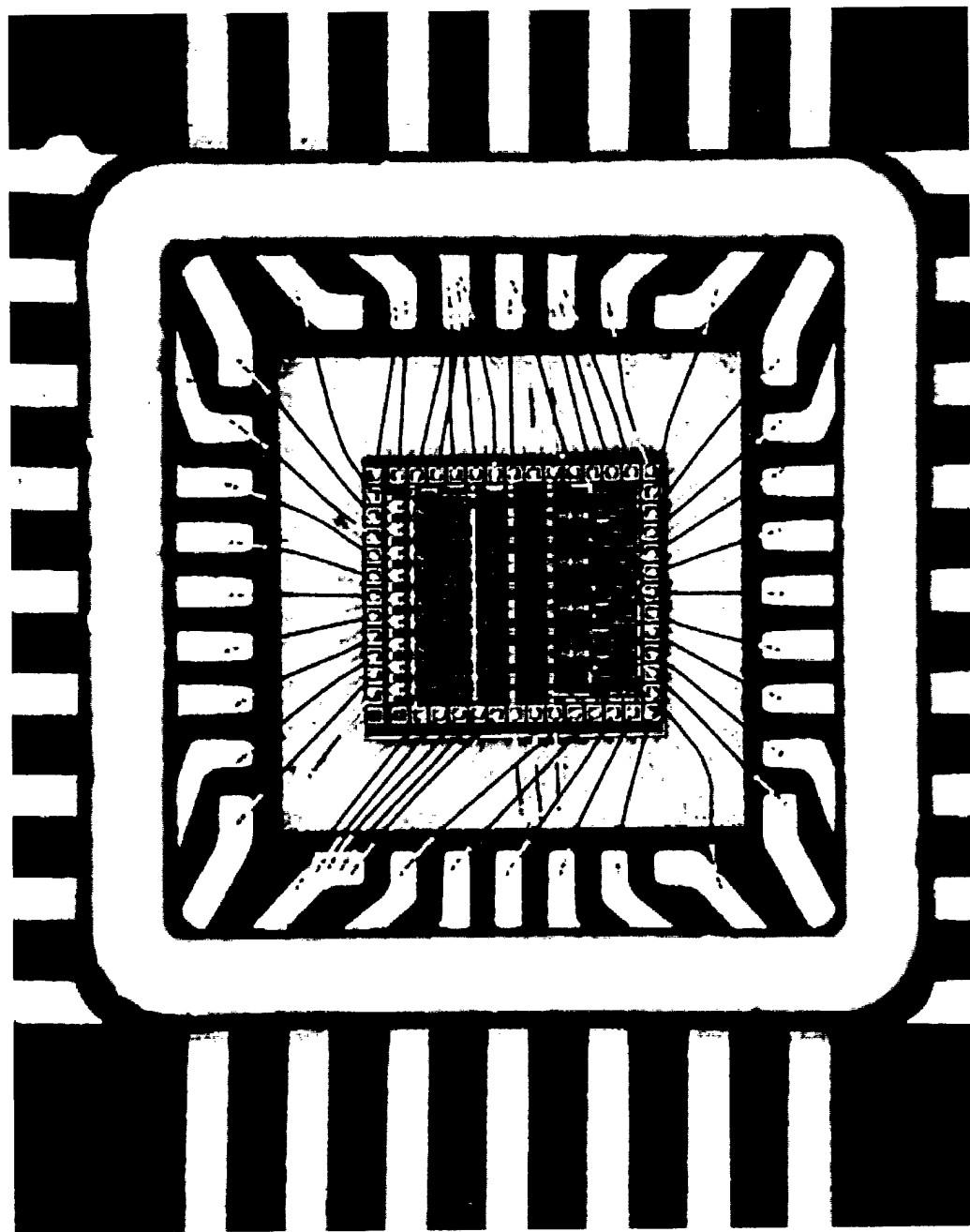
Fig.2.3.1 Packaged TIU Photograph

| Version 1a | Demux Reset Level **CML** | High Power (resistor error) |
|------------|---------------------------|------------------------------|
| Version 2a | Demux Reset Level **ECL** | High Power (resistor error) |
| Version 1b | Demux Reset Level **CML** | Low Power |
| Version 2b | Demux Reset Level **ECL** | Low Power |

Testing of packaged TIU revealed problem in the ground path for output buffers. The buffers were grounded on one side of the package and the other side was left floating. The excessive voltage drop across the bus due to its finite resistance resulted in burned traces. In the case when the chip was grounded on both sides (as in on-wafer tests) the traces did not burn out. Based on these results, the TIU ground scheme has been significantly improved and the TIU is grounded on both sides. $V_{cc}$ is also supplied from both sides of the die. These packages are currently being tested.

## 2.4 High-Speed Low Power Memory Development
## 2.4.1 GaAs MESFET TDFL Memory Circuits

This section summarizes the work completed for April through July 1996 at UCSB. A second test chip was submitted to MOSIS for fabrication in May 1996. The chip will evaluate the performance of a low switching-noise clock driver, the clock generation and distribution network, modified ECL receiver cells, and level shifters. This report also documents the test results measured from the 512x1-bit test chip submitted in January 1996.

Several sub-component changes made in the memory design have prompted us to submit a second test chip instead of the final memory design. Analysis of simultaneous switching noise (SSN) due to packaging effects showed spikes on the power rails with greater than 500 mV amplitude. Approximate values of 1 nH for bond wire and 15 nH for ceramic PGA pin inductance at 500 MHz were used. From the footprint definition and the use of

multiple bond pads and package pins, the design was found to have an effective

package inductance of 1.3 nH, 1.8 nH, and 4.3 nH per 512x1-bit for the ground, -
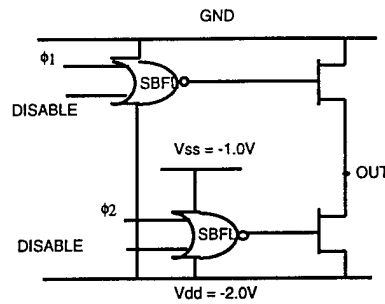
2.0 V, and -1.0 V power supplies, respectively.
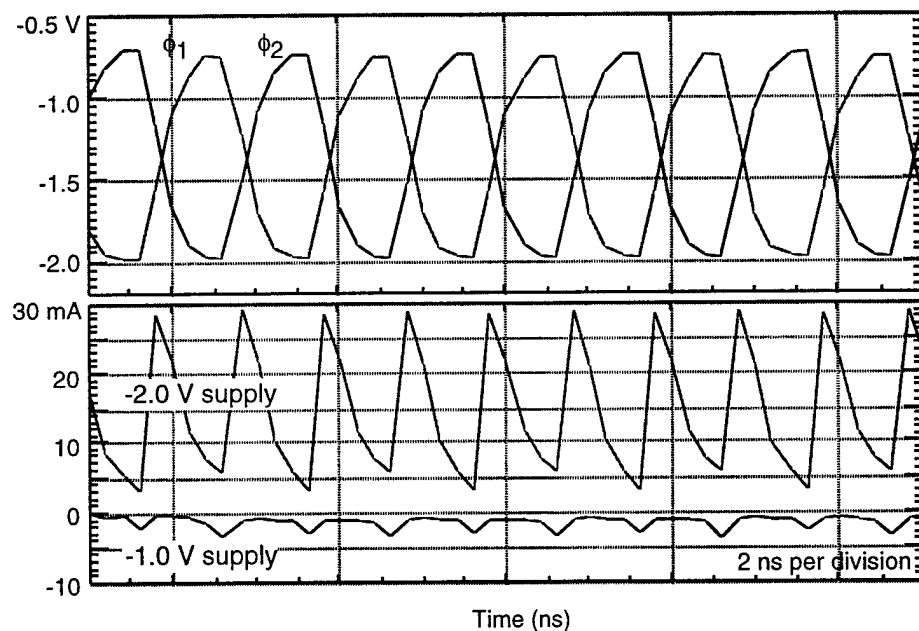
Fig. 2.4.1-1: Reduced-swing clock driver.

Fig. 2.4.1-2: Two-phase clock waveforms.

To further reduce SSN, a clock driver with controlled dI/dt characteristics

was designed, as shown in figure 2.4.1-1. The clock amplitude was reduced by

about 200 mV to 1.3 V and the rise and fall times increased to about 500 ps.

From simulations, the power/ground bounce for the new design was found to be

less than 200 mV on the ground and -1.0 V memory core supplies. Figure 2.4.1-2 shows the two-phase clock and power supply current waveforms.
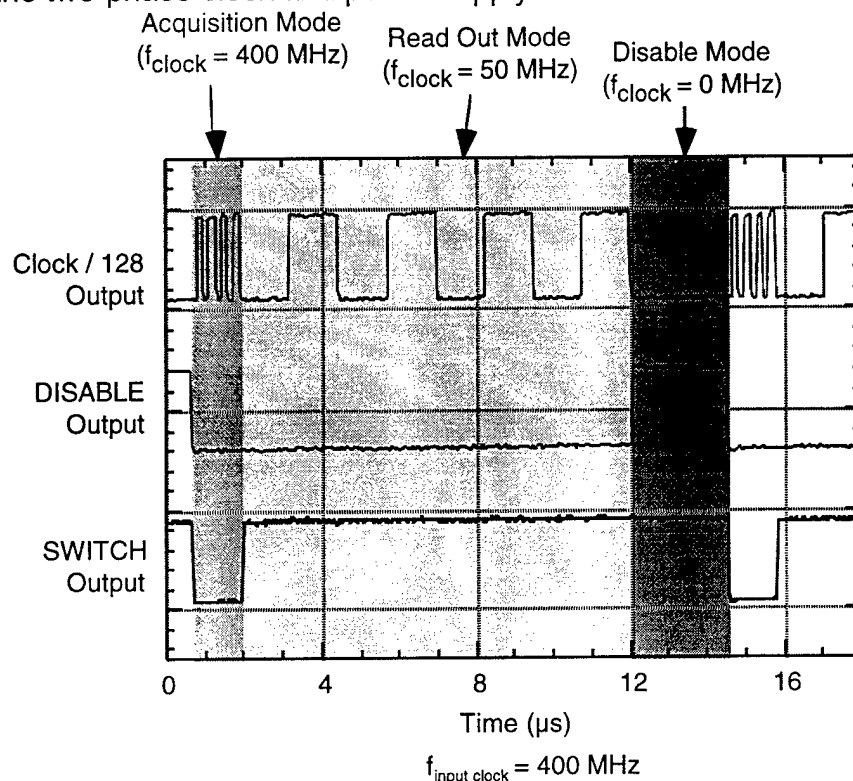


Fig. 2.4.1-3. Measurement from CLU.

The memory supply voltage levels were changed from originally proposed levels. To accommodate negative ECL interface levels, the memory core, control logic, and clock driver levels were negatively shifted by 1.0 V. This was implemented in order to preserve the supply configuration which minimizes backgating effects. The memory core and control logic will operate from -1.0 V to 0.0 V. The clock drivers will use the new ECL levels of -1.0 V to -0.0 V. The TTL output drivers remain at the same power supply levels. Backgating will not effect the memory core and slightly effect the TTL output drivers. No circuit modifications were necessary except for the ECL receivers. The standard UCSB ECL receivers were modified to output signals at -1.0 V to 0.0 V instead of -2.0 V

to -1.0 V. The receiver cell and another version which includes a static latch were submitted as part of the second test chip.

The 512x1-bit test chip submitted in January 1996 has been evaluated. The test structures included several TDFL shift registers, clock drivers, control logic, clock-data synchronization circuits, TTL output drivers, and static latches. The control logic unit (CLU) properly operated above 500 MHz. As shown for an acquisition cycle in figure 2.4.1-3, the CLU enters all three operating modes when the write enable is active: acquisition mode at 400 MHz, read out mode at 50 MHz, and standby mode. A *DISABLE* high signal takes the CLU into standby mode, while a *SWITCH* high signal takes the CLU into read out mode. However, due to a layout error on a data buffer cell, the shift registers could not be evaluated. The second test chip (May 96) includes TDFL shift registers so that the memory array can still be characterized before committing the large memory chip to fabrication. The synchronization test circuit latches the input data to phase 1 of the two-phase clock as shown in figure 2.4.1-4. The circuit operated up to 430 MHz from an off-chip clock source. A static D-flip-flip test circuit which is part of the input interface operated above 500 MHz. The TTL output drivers operated above 50 MHz while driving the package and an 8-cm PCB strip load. A 4.0 V voltage swing was observed which gives a 2.0 V output-high noise margin. The TTL driver power dissipation was 42 mW when active and 2.3 mW when disabled.

The May 1996 test chip was received on August 7th and is currently being tested. Preliminary results from several dies show 450 MHz of a 1-bit segment with 10 MHz data. The 1-bit segment includes the modified ECL receivers, 1/12th scale clock distribution net, two-phase clock drivers, input and output latches, and an 84-stage TDFL shift register.
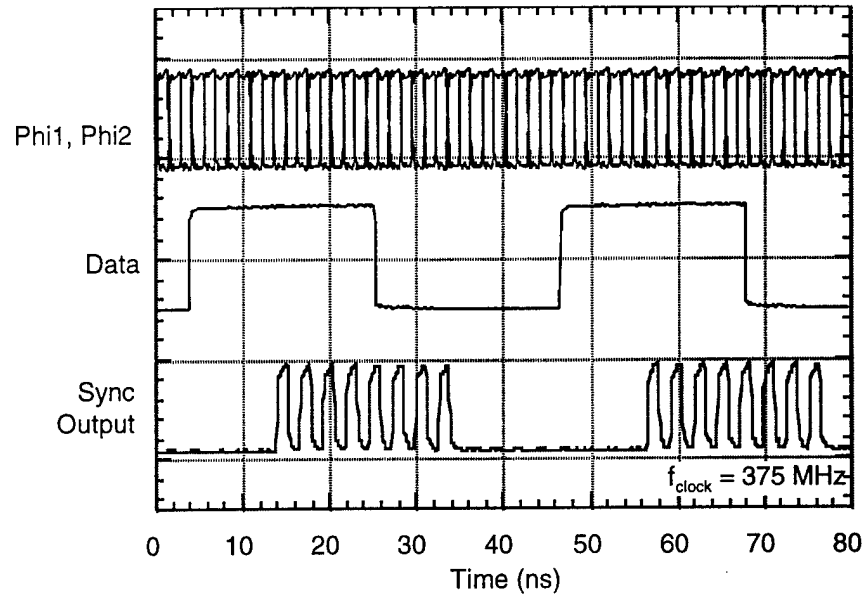
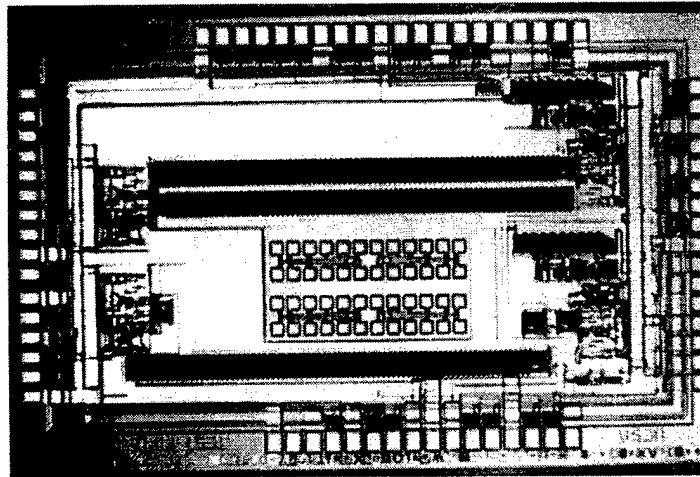Fig. 2.4.1-4: Measurement from synchronization circuit.



Fig. 2.4.1-5: Micrograph of January 1996 test chip.

## 2.4.2 High Speed CMOS Memory Circuits

Following modules have been designed and simulated for 400MHz operation.

- C2MOS memory core
- ECL to CMOS input pads
- TTL output pads (50MHz output)
- Timing logic unit
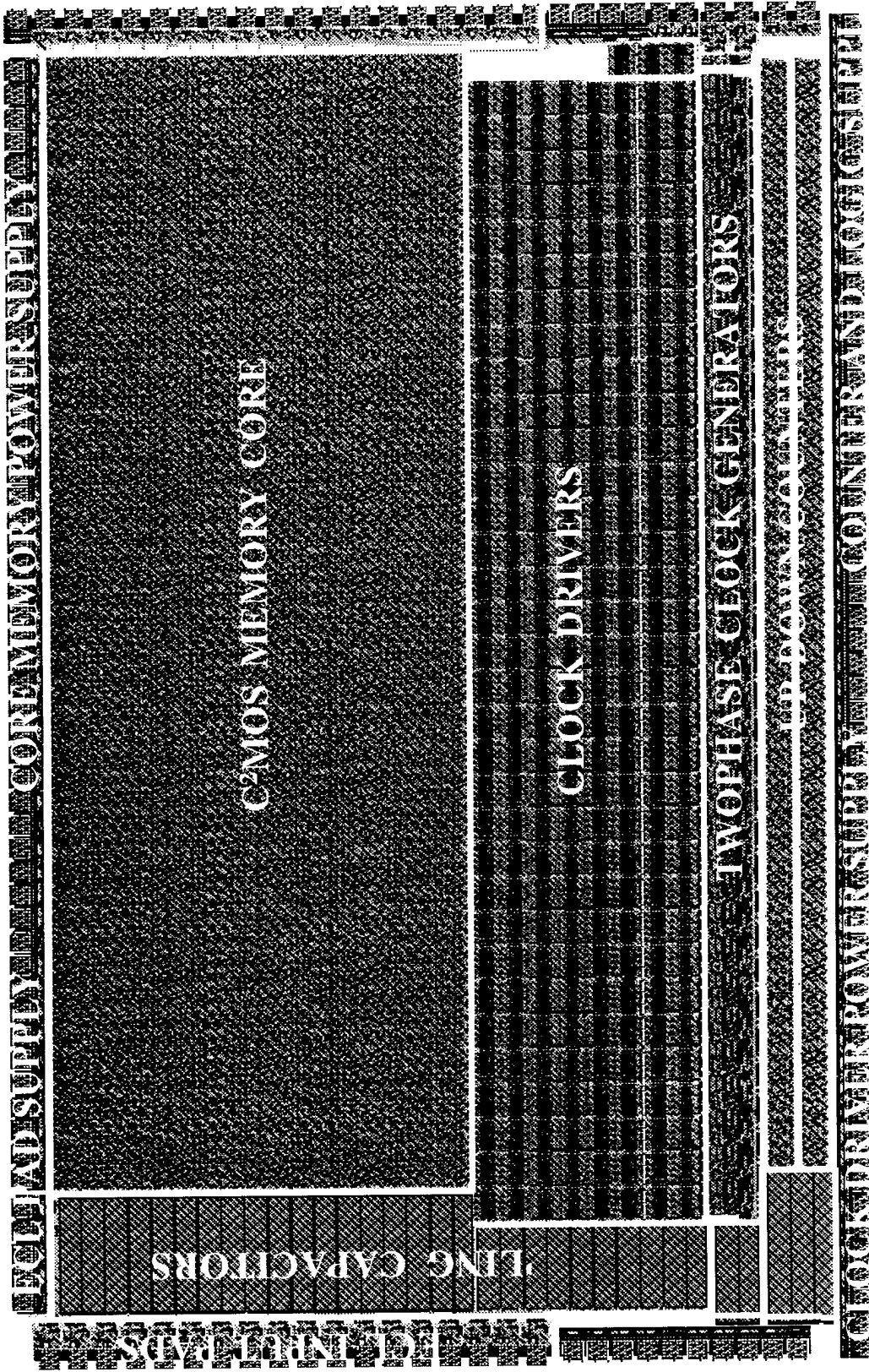- Twophase clock generators and drivers

Fig.2.4.1 Memory Layout

- Counters

The complete memory layout is now being put together and is shown in Fig.2.4.2. The layout is not completely done and should be finalized and released for fabrication in 3 months. The design specification for the memory is shown below.

- Memory Size = 18 x 512 bits
- Maximum input clock = 375MHz
- Minimum input clock = 20MHz
- Input logic level = ECL
- Output logic level = TTL
- Temperature range = 0 - 50$^{\circ}$C
- Power dissipation = 2.5W @ 375MHz
- Supplies = -2, 2 and 5V

## 3.0 Progress on Advanced Packaging with Epitaxial Layer Transfer

The status and progress of this part of the program were briefed to ONR on June 20, 1996, and August 7, 1996, to ONR and NASA personnel, respectively. This work covered the period August 1995 to February 1996. Because of a temporary funding gap no significant technical activity occurred during the last quarter.

In the program reviews we discussed the problems we encountered in adopting the low temperature process developed for the diamond-like carbon(DLC) heatspreader to a metallic bond between the GaAs circuit film and heatsink. (As discussed in previous reports, this change in technical approach became necessary because of the low thermal conductivity of current DLC).

Two main problem areas were revealed. First, the current combination of thermal resin and temporary carrier did not provide sufficient support for the GaAs circuit film during metal alloying of the film to the AlN heatsink primarily because of the softening of the thermal resin. This occurred even at the relatively low temperatures needed to alloy indium (Tm ~157$^{\circ}$C) and caused

extensive deformation of the circuit film. Second, and consequently, the planarization of the dual chip thin film module was difficult because of insufficient curing of the planarization agents (polyimide and several epoxies were evaluated) because the cure temperatures had to be kept below the melting point of indium. (Since indium is highly malleable we obtained a relatively strong bond between the GaAs circuit film and the AlN heatsink by simply cold-welding the indium metallized surfaces using pressure at room temperature).

Accordingly, our strategy is to develop a process capable of a higher temperature range (Å200°C vs. Å100°C for the current process). This will require the use of a thermal resin with a higher glass transition teperature (Tg) and a higher melting point metal for the circuit film/heatsink attach.

In the first case, we achieved partial success by using Stastick resin No. 415 (Tg ~ 180°C), but the temperature required for a robust and uniform film attach to the temporary carrier (Å 300°C) often caused film fracture due to stresses caused by differential thermal expansion.

We plan to resolve this issue by switching to a GaAs temporary carrier which will have the same thermal expansion characteristics as the circuit film although the differential expansion of the thermal resin itself may still cause sufficient stress to cause film fracture. This will need to be evaluated experimentally (for the low temperature DLC process we found borosilicate glass or porous alumina excellent temporary carriers).

Secondly , we plan to use either Pb/Sn (Tm = 183°C) or a Sn/Ag/In alloy (Tm = 187°C) to obtain a higher temperature range to allow effective curing of the planarization agents without softening the metallic bond between circuit film and AlN heatsink.

In addition, we are also evaluating alternative approaches to obtain effective thermal management of the circuit film without the use of a metal bond which has increased the proccessing complexity considerably over the original DLC proccess.

We are focusing on the potential of using "atomic" bonding between the circuit film and the AlN heatsink. Currenly atomic bonding is carried out

successfully for Si to Si (commercial products are available). However, the stringent requirements for atomic bonding ( surface smoothness better than one nanometer, flatness, surface activation, and extreme cleanliness) are currently only obtained in the Si industry with reasonable reproducibility. We plan to measure the surface roughness of the GaAs circuit film after substrate removal to obtain a initial and critical reference point as to the potential for atomic bonding for this application. We will use atomic force microscopy (AFM) to obtain detailed topological information on the circuit film backside.

## 4.0 Summary of Financial Status

| Month (1996) | Expenditure Telos | Expenditure DAS | Cumulative Expenditure to Date |
|---|---|---|---|
| April | ($1,392) | $63,342 | $61,950 |
| Cum | $548,802 | $671,270 | $1,220,072 |
| May | ($1,279) | $30,081 | $28,802 |
| Cum | $547,523 | $701,351 | $1,248,874 |
| June | $3,906 | $46,148 | $50,054 |
| Cum | $551,429 | $747,499 | $1,298,928 |

Fig. 4.0-1 through fig. 4.0-3 show the spending funding, cost+fee+comit, and forecast from 6/95 to 9/95.
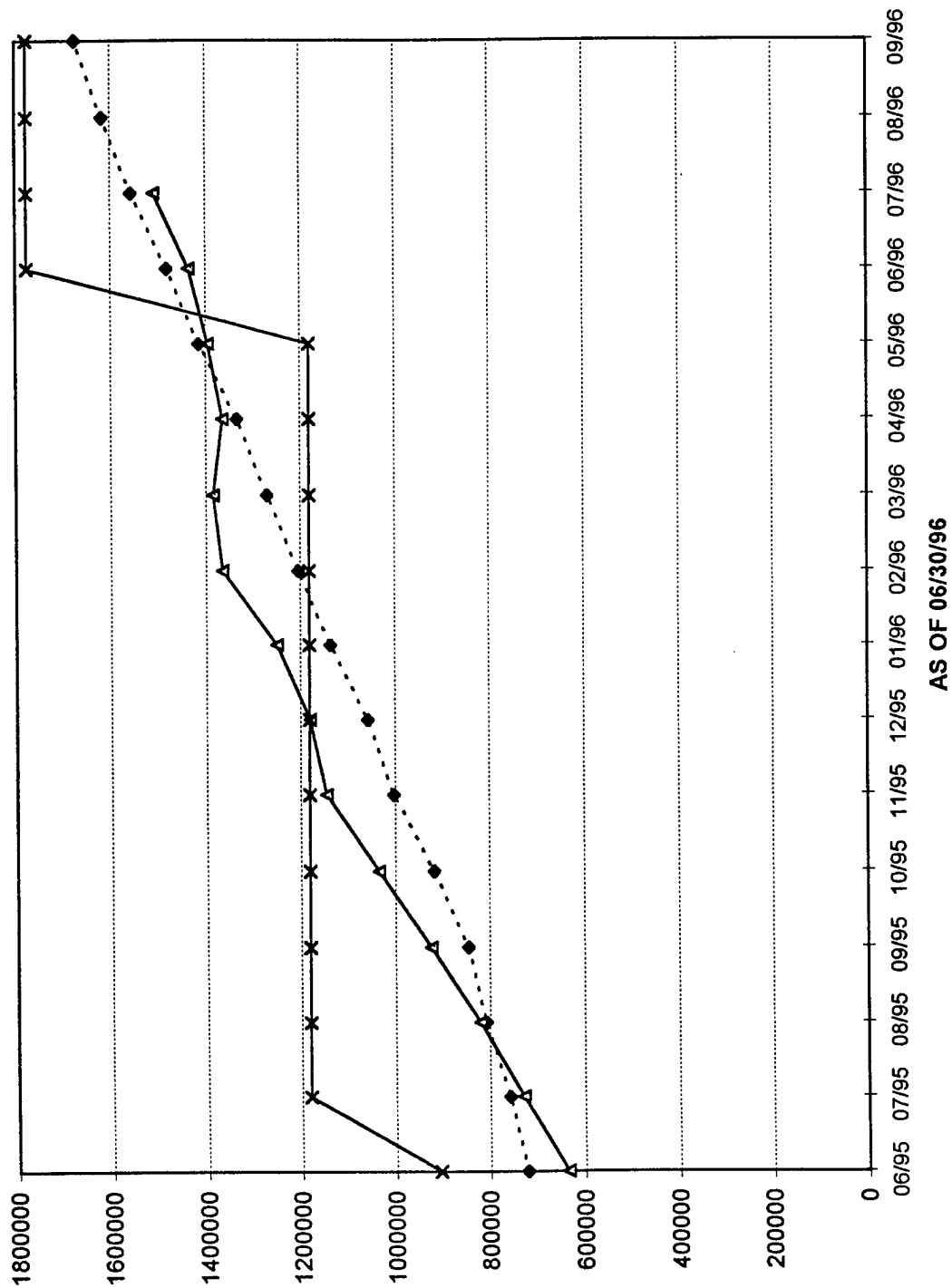
G.O. 71104 TOTAL PROGRAM

AS OF 06/30/96

FORECAST
COST+FEE+COMIT
FUNDING

Figure 4.0-1

WAVEFORM DIGITIZER (NASA)
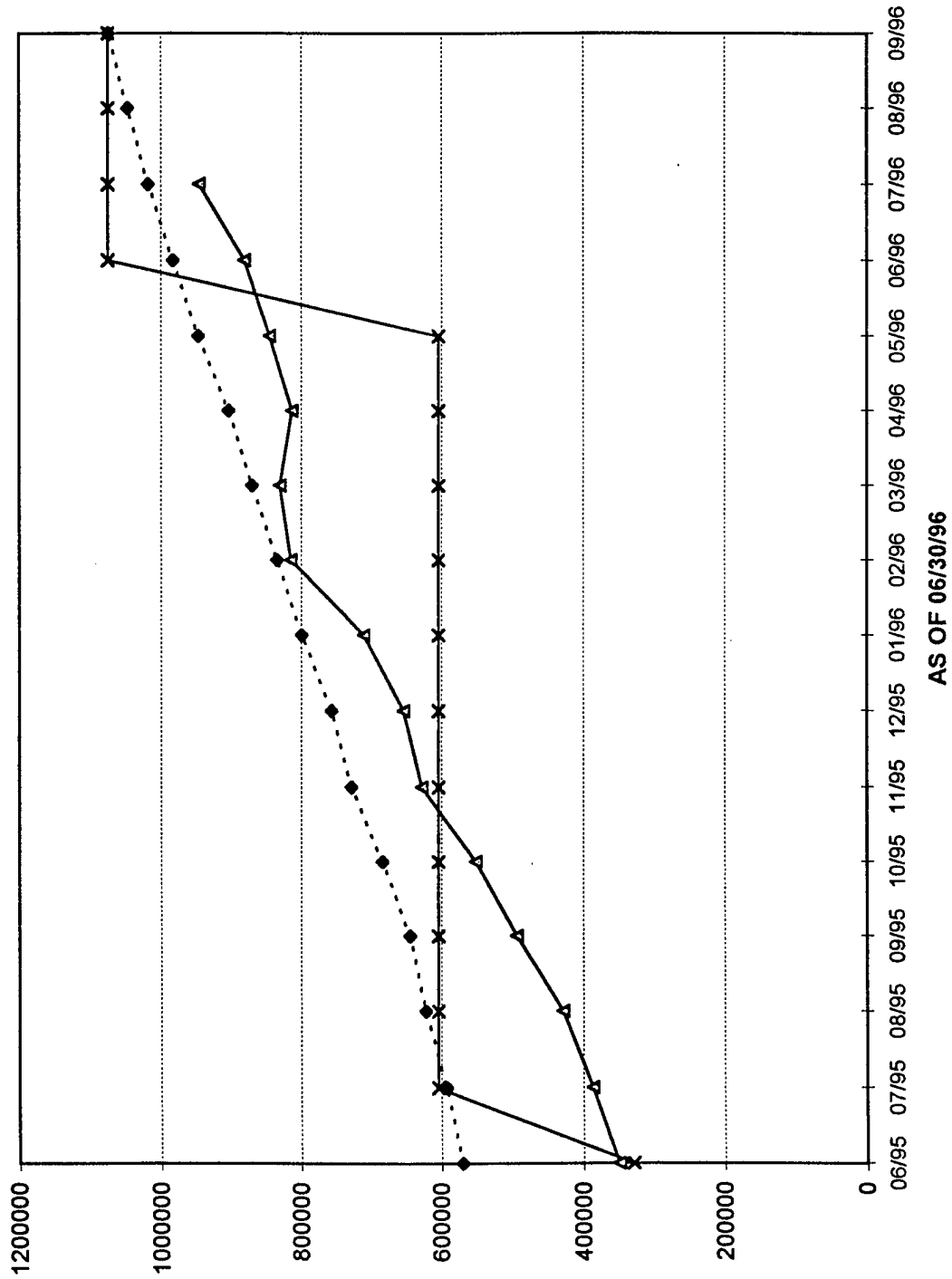G.O. 71104 SUB: 0001

FORECAST
COST+FEE+COMIT
FUNDING

AS OF 06/30/96

Figure 4.0-2

ADVANCED PACKAGING (ONR)
G.O. 71104 SUB: 0002

AS OF 06/30/96

FORECAST
COST+FEE+COMIT
FUNDING

Figure 4.0-3